IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Alan R. Reinberg

Title: METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT

Docket No.: 303.522US1
Filed: August 25, 1999
Examiner: Richard A. Booth

Serial No.: 09/382,442
Due Date: November 22, 2002
Group Art Unit: 2812

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

X   A return postcard.
X   An Amendment and Response (4 Pages).
X   A Clean Version of Pending Claims (5 pgs.).

Please consider this a **PETITION FOR EXTENSION OF TIME** for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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By: _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this _22_ day of November, 2002.

_____Tira Kohut_____
Name

_____
Signature

Customer Number 21186
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(GENERAL)

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AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

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Applicant has reviewed the Office Action mailed on August 22, 2002. Please amend the above-identified patent application as follows.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 1, 7, 26, 35, and 37. The specific amendments to individual claims are detailed in the following marked up set of claims.

1.   (Amended) A method for reducing random single bit data loss in a FLASH memory circuit having a programming operation and an erase operation, comprising:

providing a semiconductor layer having a surface;

heating the layer in an atmosphere comprising a Hydrogen isotope wherein the Hydrogen isotope is incorporated into the layer; and

fabricating a memory circuit having a programming operation and an erase operation, comprising single bit data using the semiconductor layer, the fabricating comprising fabricating a gate region in the layer; treating a portion of the surface to form a thin layer of insulator film adjacent to the gate region and under the gate region; and heating the gate region and the thin layer in an atmosphere comprising Hydrogen isotope, wherein single bit data loss is reduced and wherein random single bit data loss is prevented in both the programming operation and the erase operation.